

-60V P-Channel Power MOSFET

• **General Description**

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

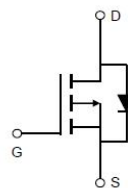
• **Features**

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- High GOX reliability
- Low Thermal resistance

• **Application**

- BLDC Motor driver
- DC-DC
- Load Switch

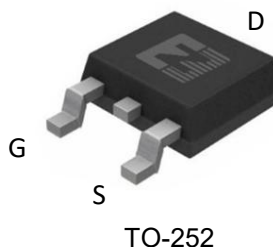
• **Product Summary**



$$V_{DS} = -60V$$

$$R_{DS(ON)} = 100m\Omega$$

$$I_D = -10A$$



• **Ordering Information:**

Part NO.	ZMA930P06D
Marking	ZM930P06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

• **Absolute Maximum Ratings** ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		-60	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	-10	A
	I_D	$T_C=75^\circ\text{C}$	-10	A
	I_D	$T_C=100^\circ\text{C}$	-8	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	-40	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	38	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.4	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=-10\text{V}$, $R_g=25\Omega$,	5	mJ
		$L=0.5\text{mH}$, $V_{GS}=-10\text{V}$, $R_g=25\Omega$,	10.5	mJ
ESD Level (HBM)	CLASS 1C			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	4	°C/W
Thermal resistance, junction-ambient ^②	R_{thJA}		-	62	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.3	-1.8	-2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-60V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5A$		100	130	m Ω
		$V_{GS}=-4.5V, I_D=-4A$		128	166	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_{SD}=-1A$		20		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=-5A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f = 1MHz, V_{DS}=-25V$	-	920	-	pF
Output capacitance	C_{oss}		-	67	-	
Reverse transfer capacitance	C_{rss}		-	44	-	
Gate Resistance	R_g	$f = 1MHz$	-	8		Ω
Total gate charge	Q_g	$V_{DD} = -15V,$ $I_D = -10A,$ $V_{GS} = -10V$	-	13	-	nC
	$Q_g(-4.5v)$		-	6	-	
Gate - Source charge	Q_{gs}		-	2.3	-	
Gate - Drain charge	Q_{gd}		-	2.4	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V,$ $R_G=3.3\Omega, I_D=-10A$	-	14	-	ns
Turn-ON Rise time	t_r		-	17	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	41	-	ns
Turn-Off Fall time	t_f		-	18	-	ns

Fig.1 Gate-Charge Characteristics

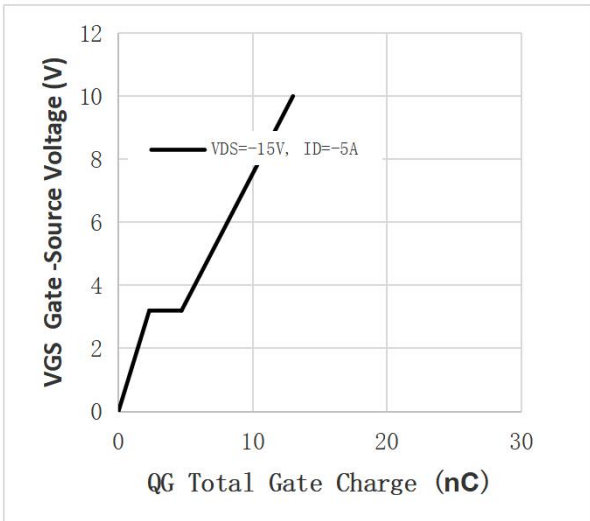


Fig.2 Capacitance Characteristics

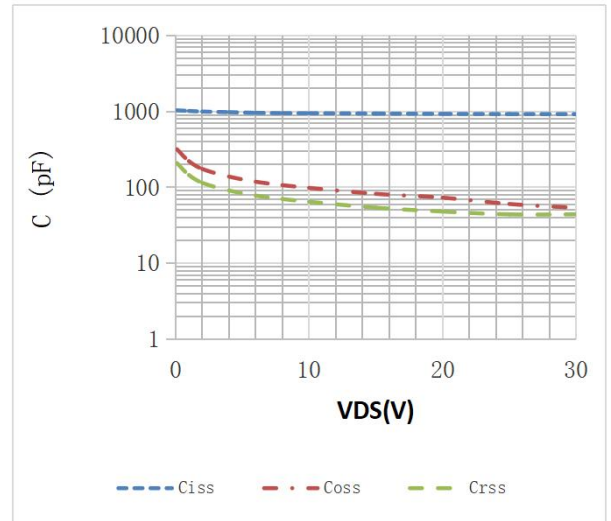


Fig.3 Power Dissipation

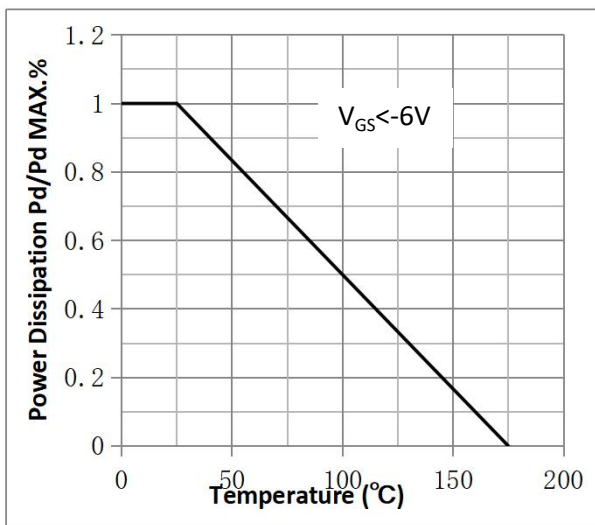


Fig.4 Typical output Characteristics

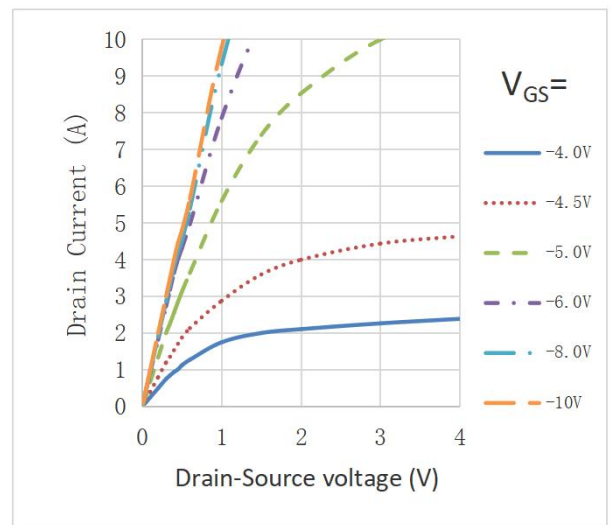


Fig.5 Threshold Voltage V.S Junction Temperature

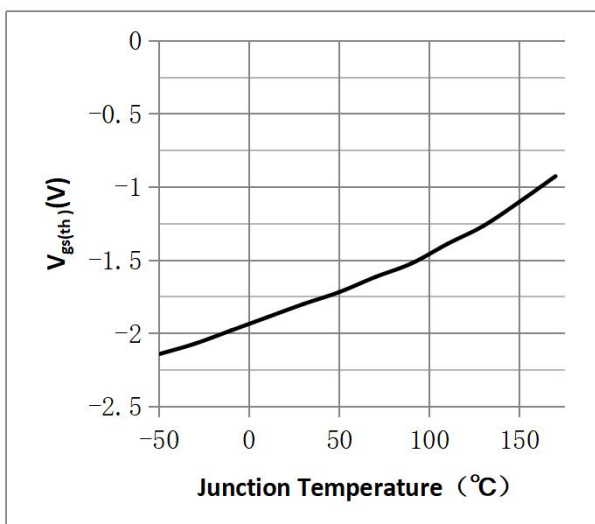


Fig.6 Resistance V.S Drain Current

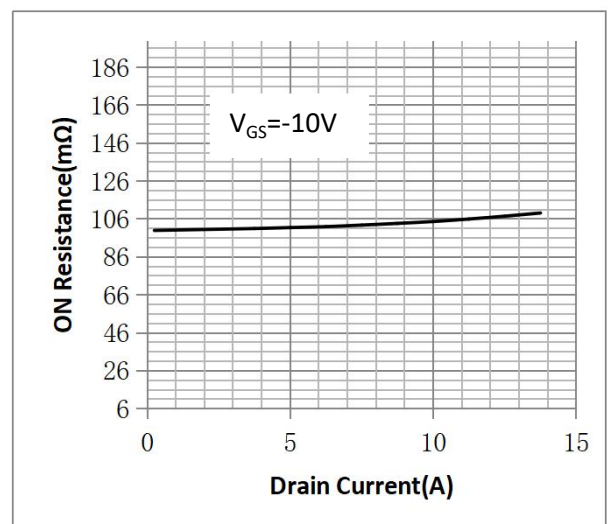


Fig.7 On-Resistance VS Gate Source Voltage

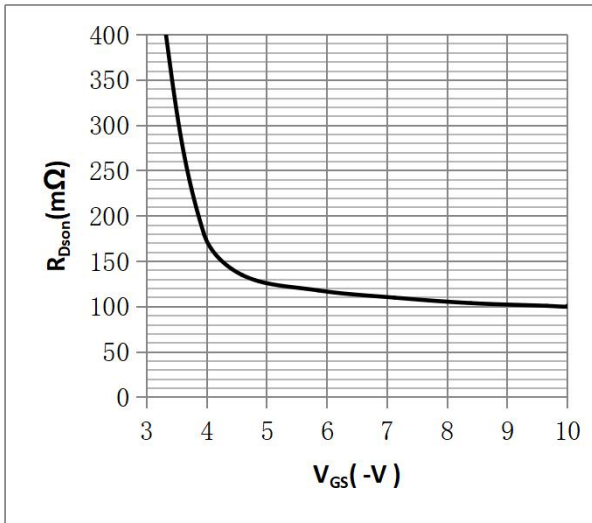


Fig.8 On-Resistance V.S Junction Temperature

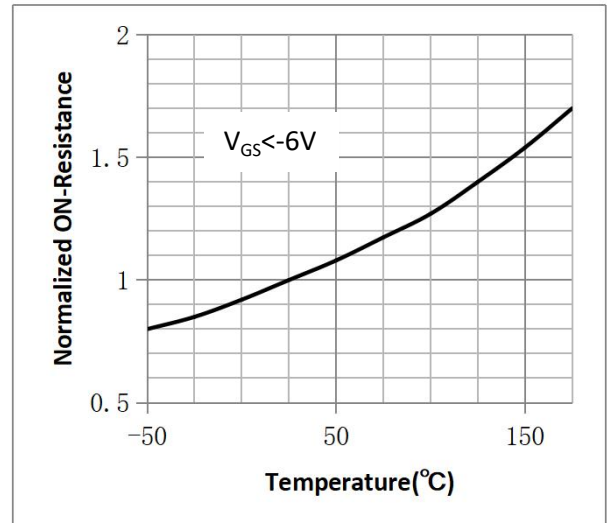


Figure 9. Diode Forward Voltage vs. Current

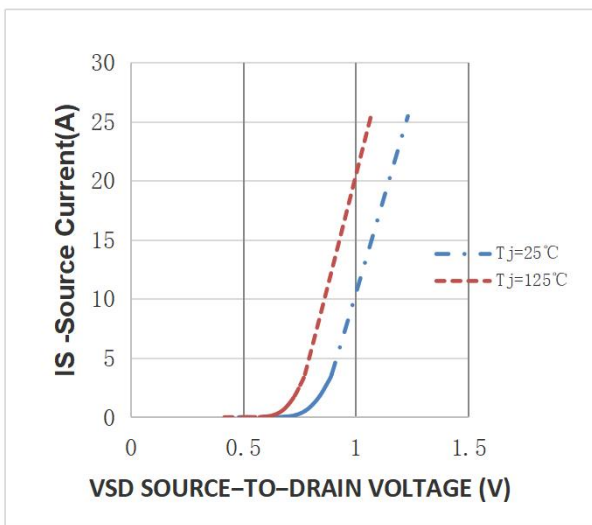


Figure 10. Transfer Characteristics

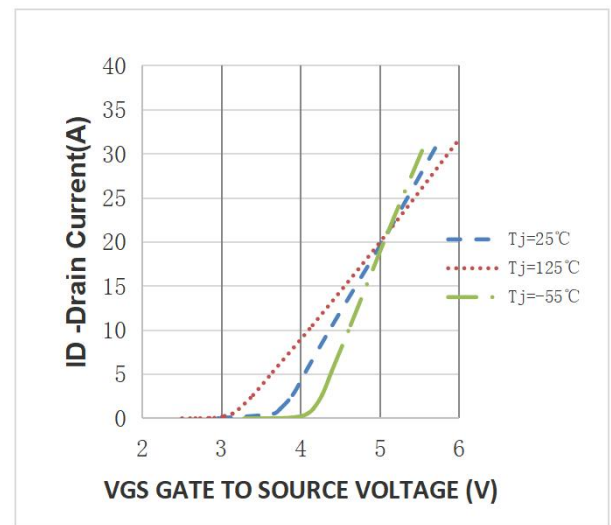


Fig.11 Safe Operating Area

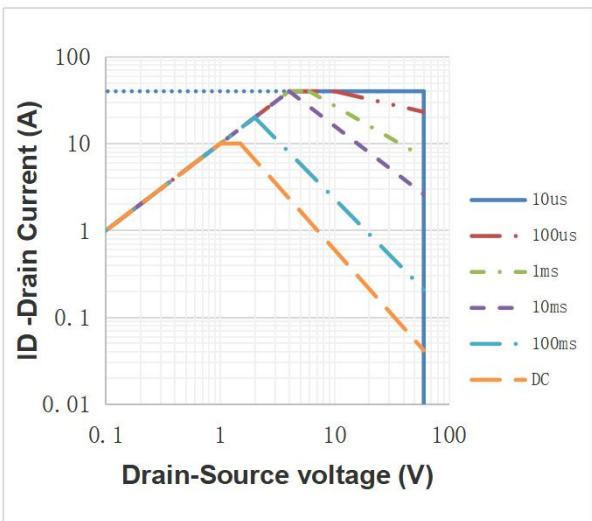
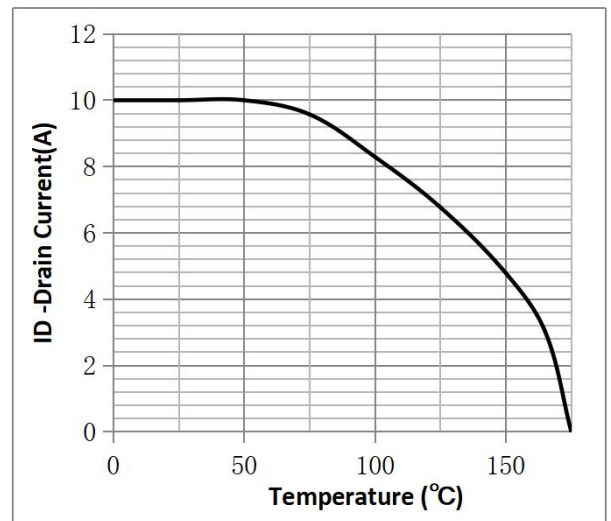
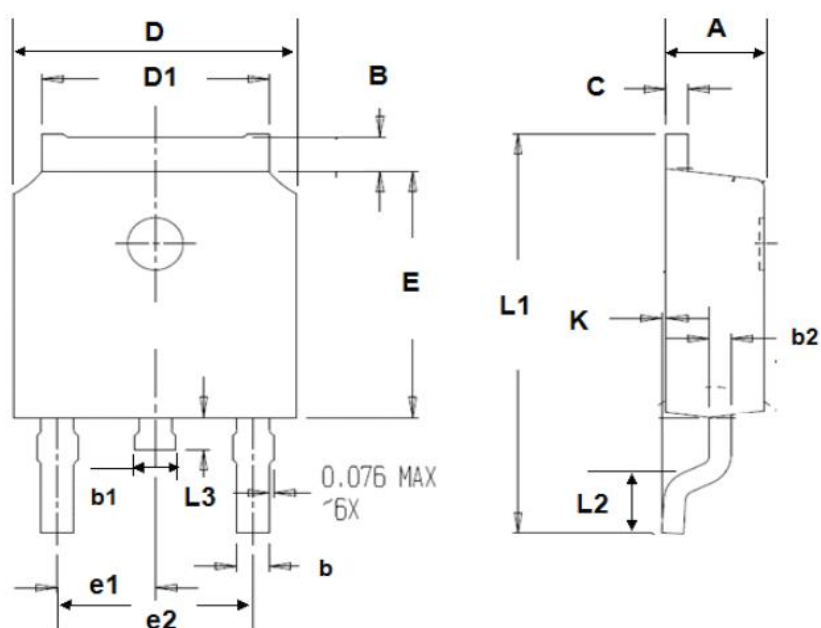


Fig.12 I_D vs. Case Temperature^③



•TO-252 Package Outline

SYMBOL	min	max	SYMBOL	min	max
A	2.10	2.50	B	0.85	1.25
b	0.50	0.90	b1	0.50	0.90
b2	0.45	0.70	C	0.45	0.70
D	6.30	6.75	D1	5.10	5.50
E	5.30	6.30	e1	2.24	2.35
L1	9.20	10.60	e2	4.43	4.75
L2	0.90	1.75	L3	0.60	1.10
K	0.00	0.23			



Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=-20V/+10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=-10V$.

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Revision History

Version	Date	Change
A	2021.11.12	NEW
B	2021.12.7	Add ESD LEVEL
C	2022.9.8	1.Add Reach, HF figure 2.ID Modify 3.Rth modified